Bimaterial electromechanical systems for a biomimetical acoustic sensor

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Bimaterial planarized micromechanical beams have been designed, simulated, and fabricated with lengths in the range 800–5800 μm and distance to substrate 0.8–4.0 μm. The beams are to be used as vertical-mode resonant gates on p-type field-effect transistors for implementing an adaptable MEMS acoustic sensor inspired by the human ear. A process for fabricating planar bilayer double-clamped beams made of silicon nitride (SiN) and aluminum (Al(1%Si)) has been developed. The planar design and bimaterial approach allow the fabrication of relatively straight beams with length up to 5800 μm with the possibility of controlling the degree of static deflection of the beams. The fabricated beams have shown a maximum deflection of ~300 nm and a transverse concave shape with respect to the substrate due to the bilayer nature of the structure. From wafer curvature measurements, the stress in the SiN and Al(1%Si) is 200 and 280 MPa, respectively. Finite element simulations and analysis of the profile of the beams have demonstrated that the films' stress magnitude influences the longitudinal and transverse profile of the beams. The fabricated devices resonate mechanically in the range 15–160 kHz. Preliminary electrical characterization of the devices has shown drain currents in the μA range for gate voltages of −20 to −25 V and drain voltages of −5 V. © *2012 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4764094]

I. INTRODUCTION

Since late 1980s, researchers have turned their attention on biomimetics as a new way of discovering unconventional designs and materials both for creating new device concepts and for solving engineering problems.[1] In our research, we aim to implement an adaptable MEMS acoustic sensor inspired by the behavior of the human ear. The human ear represents an excellent tunable acoustic sensor able to perceive sounds with relatively wide pitch and frequency range (20–20 kHz). The inner ear acts as a transducer for the acoustic input signal that is transformed from mechanical to electrical domain, filtered and decomposed into different frequency bands.[2,3] Few works have reported on the physical modeling of the cochlea using microfabrication technology.[2,4] Thus far, the MEMS microphones developed and used in the market suffer from limited tunability and directionality.

In our system, we propose an array of MEMS resonant gate transistors (RGTs) to implement an active self-adjusting acoustic sensor able to detect and filter acoustic signals in the audible frequency range (Fig. 1). The array of MEMS beams together with the active channel of the transistors acts as vibration transducers, mimicking the behavior of the basilar membrane of the human ear.[2,4] The MEMS structures are to be connected to a neuromorphic auditory analog circuit that provides feedback to the resonant gates in order to adjust the gain (sensitivity) and frequency (selectivity) of the system and consequently enable complete tunability of the device.[5]

The development of a field-effect transistor (FET) having a suspended mechanical gate shares similar issues with the integration of MEMS structures onto CMOS devices.[6] The appropriate choice of sacrificial and structural materials is essential and relatively challenging for obtaining optimal compatibility in the integration of MEMS devices with MOSFET technology. RGTs formed by a single clamped beam gate on a depletion-mode n-MOS transistor have been reported first by Nathanson *et al.* in 1967.[7] More recently, enhancement-mode n-MOS RGT designs have been fabricated with double-clamped beam gates for implementing an alternative to capacitive sensing in MEMS resonant devices operating as electrical–mechanical–electrical transducers.[8] In our work, we investigate the use of the RGTs as mechanical-to-electrical acoustic transducer with electrical feedback. In addition, we propose to utilize a p-type device rather than n-type in order to simplify and speed up the fabrication process thus enhancing and facilitating the integration with the MEMS suspended gate.

In the past, aluminum (Al) and tantalum (Ta) have been used successfully for manufacturing out-of-plane beam gates for RGTs.[9,10] However, the fabrication of relatively long beams vibrating at acoustic frequencies (length > 1000 μm) requires the ability of predicting and controlling precisely the beam's deflection and the film stress during deposition. Similar to MEMS membranes, the RGTs fabricated previously in Latif *et al.* suffer from stress issues that can lead to large static deflection and buckling thus affecting the sensitivity, reliability, and yield of the devices.[9,10] Furthermore, for the beam gates, planarized designs are preferable for reducing the number of regions with high stress concentrations thus improving the robustness and reliability of the

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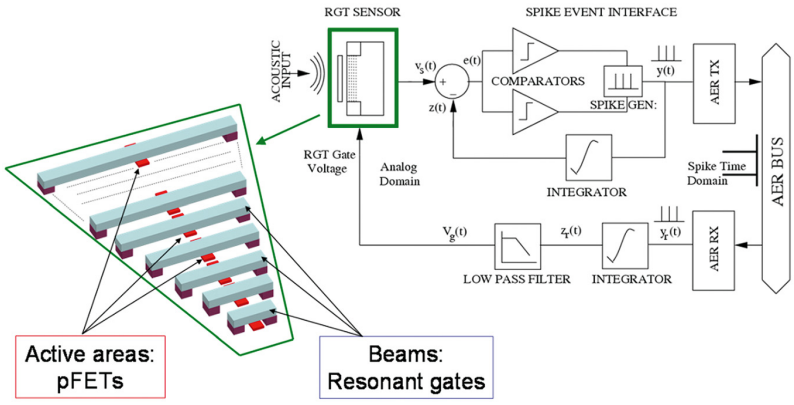

FIG. 1. (Color online) Schematic of the adaptable MEMS microphone system connected to neuromorphic circuit.

devices. In particular, in order to be used as acoustic sensors, the MEMS gates are required to possess large length (>1000 μm), small static deflection (deflection to length ratio $<10^{-3}$), and relatively low internal stress. Metallic beams with such characteristics can be fabricated by inducing tensile stress into the film using thermal cycling processes at relatively high temperatures.[11] However, the thermal cycling solution can be a critical issue when utilizing sacrificial layers that are sensitive to high temperature processes. Alternatively, the control of the deflection can be achieved using bilayer beams and exploiting the residual stress existing in the structural layers. To date, different works have reported on the evolution of the residual stress in bilayer silicon nitride (SiN) and Al MEMS structures in order to predict the electromechanical behavior of the fabricated devices and minimize unwanted bending of the structures.[12–14]

In this work, we use the bilayer approach for addressing critical aspects of structures' fabrication and solving issues associated with the internal stress of the structural layers used for implementing the devices. The bilayer approach allows the possibility of controlling the deflection of the beam thus avoiding high temperature treatments to induce tensile stress in the metallic layer forming the gate of the RGTs. In addition, the use of a bilayer design enables the possibility of engineering and controlling the static deflection of the structure,[15] which is essential for the successful fabrication of mm-long beams with a distance to substrate in the order of few μm. In particular, we use SiN as additional layer to Al for obtaining beams with an acceptable stress magnitude and an upward deflection. The choice of using SiN is justified by the fact that the film stress can be controlled by varying the process parameters during plasma-enhanced chemical-vapor-deposition (PECVD).[16] We propose to exploit the existence of residual stress in order to engineer the final deflection of the beam.

The design, fabrication, and characterization of SiN/Al(1%Si) resonant gate p-type FETs (RG-pFETs) are reported. The gates are designed as bilayer SiN/Al(1%Si) double-clamped beams (bridges) with lengths in the range 1000–5800 μm and widths of 10–50 μm. In addition, the fabrication process presented introduces the planarization of anchors' material to sacrificial layer thus allowing the development of released planarized structures with a vertical distance to the substrate controllable in a range 0.8–4.0 μm. Measurements and finite element analysis (FEA) have been performed in order to analyze the static deflection and dynamic behaviour (i.e., resonant frequency) of the bilayer structures. Particular attention has been focused on the internal stress induced into the Al(1%Si) and SiN layers during the fabrication process. The influence of the internal stress on the structures profile and resonant frequency has been examined and discussed.

II. THEORY

The static deflection of bilayers MEMS structures can be controlled by exploiting the residual stress existing in the structural materials.[15] For instance, the radius of curvature ρ of a bilayer beam can be calculated following Timoshenko's approach for bimetallic beams and can be written as[15,17]

$$\frac{1}{\rho} = \frac{6(m\sigma_2 - \sigma_1)}{h_2 E_2 [3m + K\left(n(1+n)^2\right)^{-1}]}, \tag{1}$$

where

$$K = 1 + 4mn + 6mn^2 + 4mn^3 + m^2n^4, \tag{2}$$

$$m = E_1/E_2, \tag{3}$$

$$n = h_1/h_2, \tag{4}$$

and E is the Young's modulus, h the thickness, σ the residual stress, and the indices 1 and 2 indicate the bottom and top layers forming the structure, respectively. From Eq. (1), the radius of curvature and thus the deflection of bilayer beams can be predicted and controlled. Similar to the influence on the longitudinal profile, the stress existing in the materials affects the transverse deflection and transverse shape of the beam.[18,19] The transverse bending caused by the difference in stress in the films forming a multilayer structure can represent an issue for the performance of MEMS diaphragm and membranes.[20]

III. EXPERIMENT DETAILS

A. Design and simulations

The bridges forming the gate of the RG-pFETs have been designed with beam length L in the range 1800–5800 μm and width W in the range 10–50 μm. The films' thicknesses have been designed using Eq. (1) so that the beams would exhibit a longitudinal upward deflection. Therefore, the thicknesses of 350 and 230 nm have been selected for the Al(1%Si) and SiN films, respectively, in order to obtain an upward deflection in the range 100–250 nm when the layers forming the beam exhibit stress magnitudes in the range 100–200 MPa. The distance between the beam and the substrate has been controlled in the range 0.8–4.0 μm during the fabrication process when depositing and planarizing the sacrificial layer.

The designed structures have been simulated by carrying out FEA with *CoventorWare* for investigating the profile and modal behavior of the bilayer bridges. For FEA, the Young's modulus E and the mass density ρ of Al and SiN have been set to $E_{Al} = 156$ GPa, $\rho_{Al} = 2.3$ kg/m^3 and to $E_{SiN} = 77$ GPa, $\rho_{SiN} = 2.7$ kg/m^3.

B. Fabrication

Figure 2 shows a schematic of the fabrication process flow. Fig. 2(a) shows the schematic of the source and drain areas fabricated with the following steps. A 1 -μm-thick layer of thermal field oxide (SiO_2) has been grown on a phosphorous-doped 3-inch Si wafer. The field oxide has been etched and gate oxide has been grown with a thickness of 70 nm. Source and drain have been implanted with boron (dose: 1×10^{14} ions/cm^2; energy: 30 keV). After forming the source and drain of the transistor, the gate oxide has been removed from source and drain contact areas by buffered hydrofluoric acid followed by an annealing step used for driving in the implanted boron ions. Al(1%Si) has been sputtered, patterned lithographically, reactive ion etched (RIE) with a chlorinated plasma and sintered at 435 °C to form source and drain contacts [Fig. 2(a)]. After the fabrication of source and drain, polyimide (PI) PI-2545 and PI-5878 G from *HD microsystems* has been deposited as sacrificial layer with different thickness t_{PI} in the range 0.8–4.0 μm on different wafers and cured at 200 °C for 30 min.[10] The PI sacrificial layer has been patterned using 7-μm thick photoresist and photolithography. Afterwards, the PI has been etched at 100 nm/min in RIE O_2 plasma with flow rate = 50 sccm, gas pressure = 50 mTorr, and RF power = 100 W [Fig. 2(b)]. After removing the remaining photoresist with acetone, a layer of SiO_2 has been deposited with PECVD. The oxide layer fills in the areas where the PI has been removed and is used as anchor material. In order to ensure that the SiO_2 filled in the anchor's volume defined in the PI sacrificial layer, the oxide has been deposited with a thickness t_{ox} greater than the PI's thickness t_{PI} ($t_{ox} = 1.5t_{PI}$).

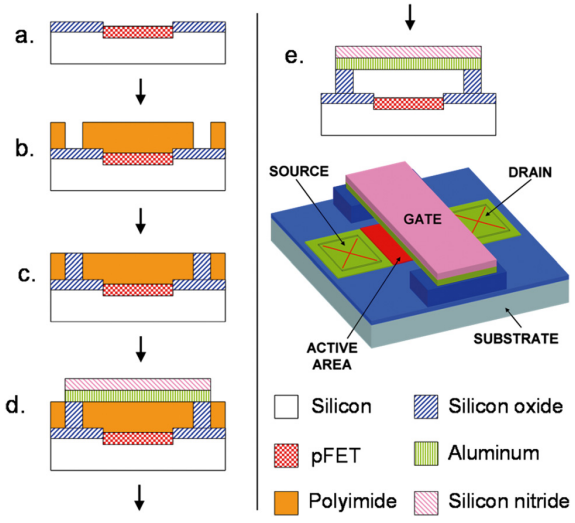

FIG. 2. (Color online) Fabrication process flow schematic and 3D schematic for Al/SiN RG-pFETs. (a) Source and drain fabrication, (b) polyimide sacrificial layer patterning, (c) silicon oxide deposition and surface planarization, (d) aluminum and silicon nitride deposition and patterning, and (e) polyimide sacrificial layer release.

At this point, the top surface of the wafer has been planarized by chemical–mechanical polishing (CMP) using silica slurry. The CMP step has been performed employing a relatively gentle process with pad speed = 35 rpm, head speed = 30 rpm, pressure = 0.4 bar, and back pressure = 0.22 bar[21] [Fig. 2(c)]. Under these conditions, removal rates of ~200 and ~75 nm/min have been obtained for the SiO_2 and PI layers, respectively. After planarization, a 350-nm-thick film of Al(1%Si) has been deposited with a magnetron sputtering tool using an Ar flow of 50 sccm, power of 1000 W, and chamber pressure of 3 mTorr. On top of the Al(1%Si) film, a 230-nm-thick SiN film has been deposited by PECVD (gases: $SiH_4 + NH_3 + N_2 + He$ with $N_2/(N_2 + He) = 40\%$; deposition temperature = 300 °C). Once the Al(1%Si) and SiN structural materials have been deposited on the planarized SiO_2 anchors' and PI sacrificial layer, the beam shapes have been patterned photolithographically followed by the etching of the SIN and Al(1%Si) in CHF_3 and $SiCl_4$ plasmas, respectively [Fig. 2(d)]. The PI sacrificial layer has been removed in O_2 downstream plasma at 220 °C with a SPD MEMSSTAR tool [Fig. 2(e)].[10,22] Figure 3(a) shows the scanning electron micrographs of one of the fabricated structures with length L of 200 μm and width of 20 μm. Figure 3(b) depicts a topography profile measured after the CMP planarization process showing a step of about ~6 nm between the SiO_2 anchor and the PI sacrificial layer.

C. Measurements

The wafer curvature has been measured after film deposition and critical process steps (i.e., high temperature 200–300 °C) for extrapolating the stress of SiN and Al(1%Si) films using Stoney's formula. These measurements have been carried out by performing separate experiments reproducing the film processing during the fabrication procedure (see Sec. III B) so that the specific fabrication step that gives rise to stress together with its magnitude could be traced back.

The planarization process has been characterized by observing the surface profile after the CMP step with a

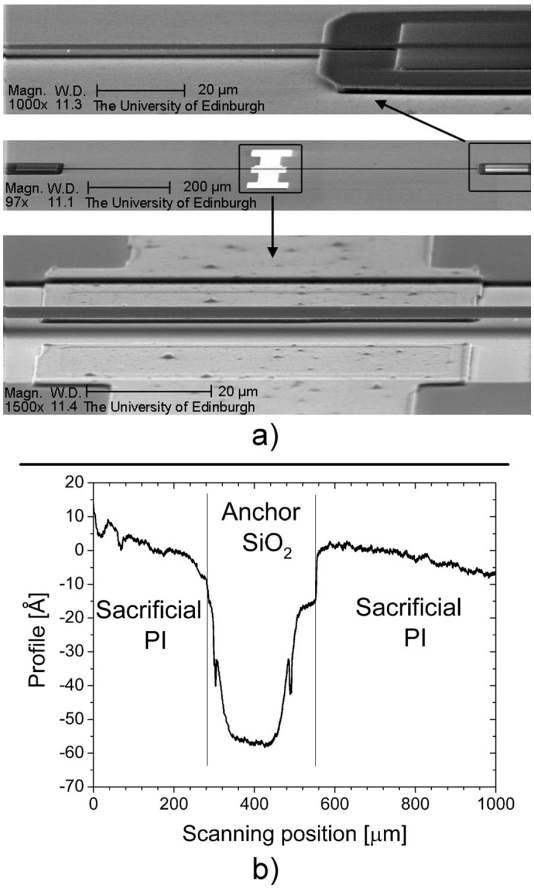

FIG. 3. (a) Scanning electron micrograph of one of the fabricated RG-pFETs. (b) Detail of surface profile after planarization.

DEKTAK profilometer. In addition, the final profile of the fabricated beam structures has been investigated with a *Zygo* white light interferometer (WLI) using a stitching technique. However, the measurement of the longitudinal profile is particularly critical due to the relatively large length to width ratio of the fabricated structures. Therefore, for beams with length $L > 2000\,\mu$m, the distance between the beam and the substrate has been measured with a separation of $300\,\mu$m between two consecutive measurements.

The mechanical resonance of the bridges has been investigated by mounting the chips containing the devices on a piezoelectric disc. Vibrations have been induced by applying an ac voltage across the piezoelectric disc and therefore transferred to the bridges (mechanical actuation). A relatively low actuation voltage peak-to-peak magnitude of 0.2 V has been applied to the piezoelectric disc to prevent the beams from contacting the substrate. The resonant frequency of the fabricated structures when actuated mechanically has been measured in vacuum (~0.001 mbar) with a *Polytec* laser vibrometer.[9]

Preliminary dc electrical measurements have been performed on the final integrated RG-pFET devices. In particular, the drain current I_{DS} has been measured as a function of drain to source voltage V_{DS} for different gate to source voltages V_{GS} using a *Hewlett Packard 4156B* semiconductor parameter analyzer. For these measurements, the source and substrate have been grounded and the drain and gate voltages have been varied.

IV. RESULTS AND DISCUSSION

A. Static characterization

1. Stress

The residual stress existing in MEMS diaphragm and membranes to be used for acoustic sensors affects the sensitivity of the device. As discussed in Sec. III C, wafer curvature measurements have been carried out in order to understand the effect of the fabrication process steps on the stress of the films forming the bilayer structures. In particular, the stress of the SiN and Al(1%Si) films has been investigated after sputtering, PECVD, and release processing steps.

The measurements have shown that the as-sputtered Al(1%Si) and as-deposited SiN films are under tensile stress with magnitudes of ~+40 and ~+200 MPa, respectively. However, the Al(1%Si) film is subjected to thermal cycling when being loaded in the PECVD tool for the deposition of SiN. During the PECVD step, the Al(1%Si) film experiences an almost instantaneous rise of temperature from ~23 to 300 °C and then is held at 300 °C for 10 min. The curvature measurements performed on test wafers experiencing these temperature gradients have revealed that the Al(1%Si) stress increases to ~+280 MPa after PECVD of SiN. The stress magnitude obtained is in consistent agreement with previous studies on the effect of thermal cycling on Al(1%Si) film stress.[11] A further confirmation of the value of +280 MPa for the stress induced in the Al(1%Si) film has been given by additional curvature measurements on wafers where SiN has been deposited on a layer of Al(1%Si). Finally, when heating the films to 200 °C for the release of the sacrificial layer, the stress of SiN and Al(1%Si) has been shown to remain constant thus indicating that the films' stress is developed mainly during sputtering and PECVD process steps.

2. Deflection along longitudinal axis

Figure 4 shows the distance between the beam and the substrate measured along the longitudinal axis for the devices fabricated with length L in the range 1800–5800 μm and width of 10 μm. The beams have been shown to deflect upwards with a maximum curvature observed toward the centre of the beam. A maximum deflection of 400 nm has been measured for the longer beams with length L in the range 3400–5800 μm (deflection to length ratio in the range $1.2–0.7 \cdot \times 10^{-4}$). The distance to substrate and the maximum deflection measured show that the beams fabricated with a length/width ratio up to 580 possess a relatively straight longitudinal profile. From Fig. 4, it can be seen that the distance to substrate varies for different beams due to the varying thickness of the PI sacrificial layer throughout the wafer. This effect is due to the CMP process that results in the planarization of the topography of the wafer but it is

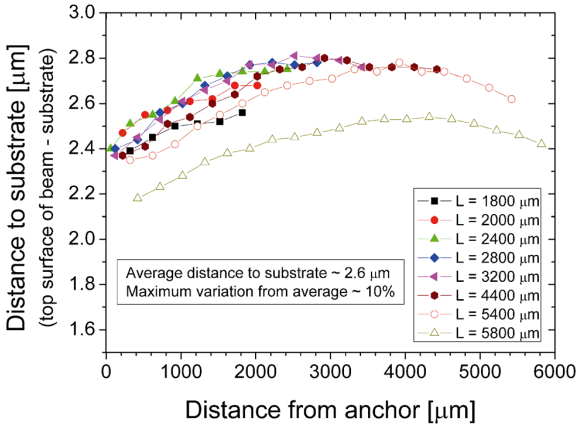

FIG. 4. (Color online) Longitudinal profile: measured distance between beams and substrate along the beam length.

influenced by the initial thickness variations of the PI sacrificial layer. The distance to the substrate, measured at the intersection between the structure's anchor and the beam, varies of ~200 nm for the different structures fabricated on a 3-inch wafer. Due to the relatively large beam lengths, the variation of the sacrificial layer thickness after planarization is noticeable also as an increase of the distance to substrate as moving along the longitudinal axis of the beam (i.e., from one anchor to the other).

3. Deflection along transverse axis

In addition to the longitudinal profile, further investigations have been carried out on the transverse profile of the structures. From SEM observations and WLI measurements, the bridges have been found to possess a transverse deflection that is more evident and relatively large for beam width $W \geq 30\,\mu$m. Figure 5(a) shows the transverse deflection measured along the beam length and a snapshot of the WLI measurement of the device. It can be seen that the transverse curvature of the structures is constant along the beam length. In addition, FEA has shown that the edge deflection increases as the beam width increases in agreement with the fact that this effect is more evident for wider beams. As discussed in Sec. II, the transverse bending observed is due to the bilayer nature of the structures.[18,19] Figure 5(b) shows the transverse profile of the fabricated structures measured with WLI ($L = 3400$ and $W = 20\,\mu$m).

FEA simulations have been performed for investigating further the influence of the films' residual stress on the profile of the fabricated bridges. In these simulations, the stress of the SiN film has been fixed at +200 MPa while the stress of the Al(1%Si) layer has been varied between +10 and +300 MPa. Figure 5(c) shows the simulated beam profile along the longitudinal and transverse axis for beam length L of 3400 μm and width W of 20 μm. From Fig. 5(c), for relative low values of tensile stress (<100 MPa) in the Al(1%Si) layer, the bilayer structure experiences an upward transverse curvature. When the stress is larger than +100 MPa, the beam curvature switches downwards with the edge deflection observed to increase as the stress in the Al(1%Si) film increases. For a stress of +300 MPa, the simulated transverse deflection is observed to be asymmetrical with respect to the longitudinal axis. This result agrees with the profiles observed with WLI measurements [see Fig. 5(a)] thus

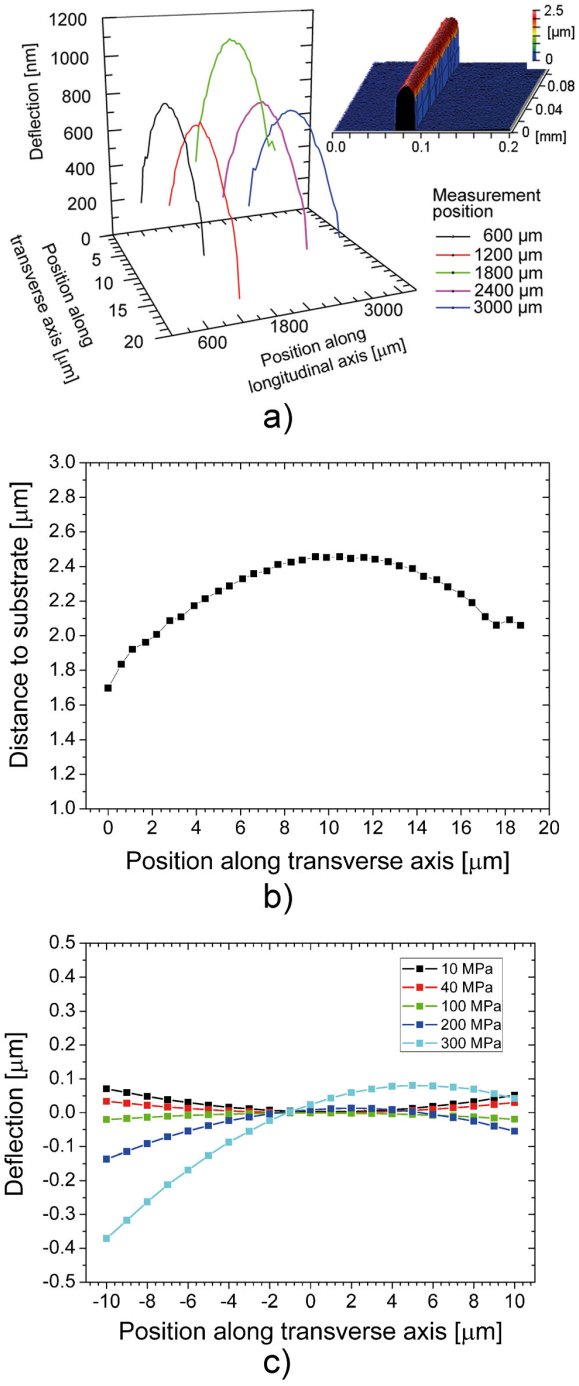

FIG. 5. (a) (Color online) White light interferometer snapshot and measured transverse profile along beam (beam with L = 3400 μm and W = 20 μm). (b) Measured transverse profile (beam with L = 3400 μm and W = 20 μm). (c) (Color online) Simulated transverse profile (beam with L = 3400 μm and W = 20 μm, Al(1%Si) stress = 10–300 MPa, SiN stress = 200 MPa).

confirming that the Al(1%Si) experiences a relatively high tensile stress (>+200 MPa). It is likely that the asymmetrical transverse deflection is due to the different Poisson ratios exhibited by the SiN and Al(1%Si).

B. Modal characterization

Figure 6 shows the simulation and measurement results for the resonant frequency of the fabricated devices as a function of the beam length. Figure 6(a) shows the resonant peaks measured at ~91 and ~26 kHz for some of the fabricated structures with length $L = 1620\ \mu$m and $L = 4420\ \mu$m. Figure 6(b) shows the measured and simulated resonant frequencies. Frequency values in the range 15–160 kHz have been measured for beams with length L in the range 800–5800 μm. The devices have been simulated using internal tensile stress magnitudes of +200 and +280 MPa measured for the SiN and Al(1%Si) layers, respectively. The difference between simulated and measured frequencies observed in Fig. 6(b) is most likely to be due to the variations in the device parameters arising from the fabrication process, such as structures thickness and materials properties. The beams' Q factor has been observed to increase from 30 to 350 as the resonant frequency increases, in consistent agreement with previous literature work that investigated the dependence of Q factor on beam geometry.[23,24]

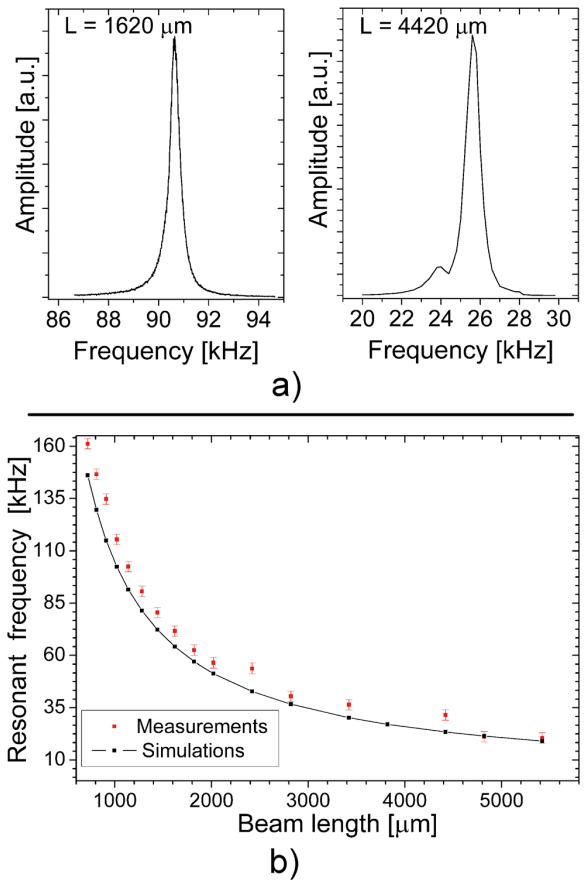

FIG. 6. (a) Measured resonant frequency peaks for beams with L = 1620 μm and L = 4420 μm. (b) (Color online) Measured and simulated resonant frequency.

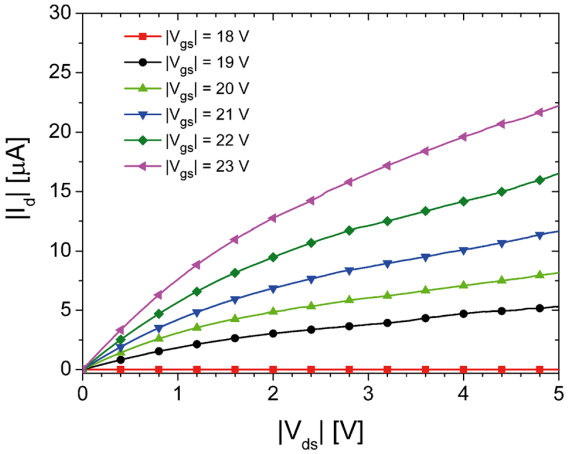

FIG. 7. (Color online) I-V characteristic measured for one of the fabricated RG-pFETs.

C. Electrical characterization

Figure 7 shows the I-V characteristic (absolute values of I_{DS}, V_{DS}, and V_{GS}) measured for one of the fabricated RG-pFETs having a gate to substrate distance $d_{G\text{-}SUB}$ of ~1.3 μm. For this device, a threshold voltage V_{th} of about −18 V has been measured. Drain currents with magnitude in the range 5–25 μA have been measured when applying a drain-source voltage $|V_{DS}|$ of 5 V and gate-source voltage $|V_{GS}|$ between 19 and 23 V. These results are in good agreement with previous measurements performed on RG-pFETs made with Ta gates and having a gate to substrate distance $d_{G\text{-}SUB}$ of 1.9 μm.[7]

The measurements performed on different RG-pFETs fabricated on the same wafer (i.e., same $d_{G\text{-}SUB}$) have similar threshold voltages and I-V characteristics showing similar drain currents at same bias voltages.

V. CONCLUSIONS

The design and fabrication of planarized bilayer SiN/Al(1%Si) double-clamped beams with length in the range 800–5800 μm (length to width ratio of 580) have been presented. The planarized SiN/Al(1%Si) beams, fabricated using PI and SiO_2 films as sacrificial layer and anchor's material, respectively, have been used for implementing the suspended gate on p-type field-effect transistors. In the fabrication process developed, during the SiN deposition, the Al(1%Si) film undergoes a thermal cycle used for burning-in the stress of the Al(1%Si) layer. The SiN layer is used for increasing the stiffness of the whole structure in order to fabricate straight beams with length up to 5800 μm. The planarization process has been developed to reduce the number highly concentrated stress regions in nonplanarized beams

while the bilayer design has been used to enable the control of the static deflection in the fabricated structures.

The fabricated bridges have been shown to possess a relatively straight longitudinal profile with a maximum deflection of 400 nm (deflection to length ratio $\sim 10^{-4}$) and distance to substrate comprised between 0.8 and 4.0 μm defined during the sacrificial layer deposition and/or planarization steps. Resonant frequencies in the range 15–160 kHz have been detected. The comparison between experimental results and FEA has confirmed stress magnitudes of +280 MPa for the Al(1%Si) and +200 MPa for SiN films, as obtained from wafer curvature measurements. Preliminary dc measurements have been performed in order to prove the electrical operation of the RG-pFETs. Drain currents with magnitudes in the μA range have been measured when biasing the suspended gates with voltages from −20 to −25 V and applying drain to source voltages of −5 V.

[1]J. F. V. Vincent, Proc. Inst. Mech. Eng., Part H: J. Eng. Med. **223**, 919 (2009).
[2]M. J. Wittbrodt, C. R. Steele, and S. Puria, Audiol. Neuro-Otol. **11**, 104 (2006).
[3]D. Haronian and N. C. MacDonald, *The 8th International Conference on Transducers '95*, Stockholm, Sweden (IEEE, 1995), Vol. 2, p. 708.
[4]R. D. White and K. Grosh, *Proceedings of IMECE'02, ASME International Mechanical Engineering Congress and Exposition*, New Orleans, Louisiana, IMECE2002-33309, 2002.
[5]T. Koickal, R. Latif, L. Gouveia, E. Mastropaolo, S. Wang, A. Hamilton, R. Cheung, M. Newton, and L. Smith, *2011 IEEE International Symposium on Circuits Systems (ISCAS)*, Rio de Janeiro (IEEE, 2011), p. 2465.
[6]O. Soeraasen and J. E. Ramstad, Microsyst. Technol. **14**, 895 (2008).
[7]H. C. Nathanson, W. E. Newell, R. A. Wickstrom, and J. R. Davis, Jr., IEEE Trans. Electron Devices **14**, 117 (1967).
[8]N. Abelé, K. Séguéni, K. Boucart, F. Casset, B. Legrand, L. Buchaillot, P. Ancey, and A. M. Ionescu, *19th IEEE International Conference on Microelectromechanical Systems (MEMS 2006)*, Istanbul (IEEE, 2006), p. 882.
[9]R. Latif, E. Mastropaolo, A. Bunting, R. Cheung, T. Koickal, A. Hamilton, M. Newton, and L. Smith, J. Vac. Sci. Technol. B **29**, 06FE05 (2011).
[10]R. Latif, E. Mastropaolo, A. Bunting, R. Cheung, T. Koickal, A. Hamilton, M. Newton, and L. Smith, J. Vac. Sci. Technol. B **28**, C6N1 (2010).
[11]D. S. Gardner and P. A. Flinn, IEEE Trans. Electron Devices **35**, 2160 (1988).
[12]S. Huang and X. Zhang, J. Micromech. Microeng. **17**, 1211 (2007).
[13]M. T.-K. Hou and R. Chen, J. Micromech. Microeng. **13**, 141 (2003).
[14]I.-K. Lin, X. Zhang, and Y. Zhang, J. Micromech. Microeng. **19**, 085010 (2009).
[15]M. W. Judy, Y.-H. Cho, R. T. Howe, and A. Pisano, *Proceedings of the IEEE Microelectromechanical Systems (MEMS 1991)* (IEEE, 1991), p. 51.
[16]K. D. Mackenzie, B. Reelfs, M. W. DeVre, R. Westerman, and D. J. Johnson, *International Conference on Compound Semiconductor Manufacturing Technology* (CS ManTech), 12.4, 2004.
[17]S. Timoshenko, J. Opt. Soc. Am. **11**, 233 (1925).
[18]T. Matsuura, M. Taguchi, K. Kawata, and K. Tsutsumi, Sens. Actuators, A **60**, 197 (1997).
[19]M. T.-K. Hou and R. Chen, J. Micromech. Microeng. **13**, 171 (2003).
[20]R. E. Strawser, K. D. Leedy, R. Cortez, J. L. Ebel, S. R. Dooley, C. F. H. Abell, and V. M. Bright, Sens. Actuators, A **134**, 600 (2007).
[21]M. Fernandez-Bolaños, N. Abelé, V. Pott, D. Bouvet, G. A. Racine, J. M. Quero, and A. M. Ionescu, Microelectron. Eng. **83**, 1185 (2006).
[22]See http://www.memsstar.com for information about oxygen downstream plasma.
[23]R. Sandberg, K. Molhave, A. Boisen, and W. Svendsen, J. Micromech. Microeng. **15**, 2249 (2005).
[24]F. R. Blom, S. Bouwstra, M. Elwenspoek, and J. H. J. Fluitman, J. Vac. Sci. Technol. B **10**, 19 (1992).